REMARKS

This response amends the Specification, the claims, the Abstract, and the Figures. More specifically, Claim 21 is cancelled and Claims 1, 5, 10, and 14, are amended to correct ministerial errors identified by the Examiner. Claim 1 is further amended to clarify Applicants' inventive contribution to the art. The claim amendments are not meant to address any art rejection and therefore, Applicants understand that any further rejection of Claims 1-20 under new art is to be non-final.

The amendment to the Specification and the Figures correct typographical errors identified by the Examiner. The amendment to the Abstract is meant to more precisely recite the technical disclosure of the application. Now in the application are Claims 1-20 of which Claims 1, 10, and 19 are independent. No new matter is added and no new issues are raised.

Objection to the Specification:

A. The Abstract:

The Abstract is objected to because it is to short and repeats information given in the title. Accordingly, Applicant amends the abstract to lengthen this paragraph to within the desired range as identified in MPEP §608.01(b). Further, Applicants' contend that the language of the abstract is clear and concise although it repeats information given in the title of the application. Therefore, the title is also clear and precise. Applicants' further note that MPEP §608.01(b) states that repeating information given in a title is permissive although not desirable. Nevertheless, Applicants' contend that the instant abstract is a concise statement of the technical disclosure of the patent application and further includes that which is new in the art to which the invention pertains. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the objection to the Abstract.

B. The Specification:

The Specification stands rejected for various typographical errors as identified on page 2 and 3 of the Office Action. The above amendment amends the Specification to correct the various typographical errors identified by the Examiner. Accordingly, Applicants' respectfully request the Examiner to reconsider and withdraw the objection to the specification.

Objection to the Drawings:

The drawings stand objected to for a number of informalities as identified on page 3 of the Office Action. Applicants' enclose herewith proposed drawing corrections to correct those identified drawing informalities and further request the Examiner to reconsider and withdraw the objection to the drawings for minor informalities.

The drawings are further objected to under 37 CFR § 1.83(a). The above amendment cancels Claim 21 and therefore Applicants' respectfully request the Examiner to reconsider and withdraw the objection to the drawings under 37 CFR § 1.83(a).

Claim Objections:

Claims 10 and 21 stand objected to for certain ministerial errors identified on page 4 of the Office Action. The above amendment amends Claim 10 to correct the identified ministerial errors and cancels Claim 21. Accordingly, Applicants' respectfully request the Examiner to reconsider and withdraw the claim objections to Claim 10 and 21.

Claim Rejections under 35 U.S.C. § 112

A. Claim Rejections under 35 U.S.C.§112, second paragraph:

Claims 5 and 14 stand rejected under 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter which the Applicants' regard as their invention. More specifically, Claims 5 and 14 stand rejected because the phrase "the mappings" in each claim lacks proper antecedent basis. Accordingly, Applicants' amend Claims 5 and 14 to provide the proper antecedent basis for the feature "mappings". Therefore, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 5 and 14 under 35 U.S.C. § 112, second paragraph.

B. Claim Rejections under 35 U.S.C.§112, first paragraph:

Claim 21 stands rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the enablement and requirement. The above amendment cancels Claim 21 and therefore Applicants' respectfully request the Examiner to reconsider and withdraw the rejection of Claim 21 under 35 U.S.C. § 112, first paragraph.

Claim Rejections under 35 U.S.C. § 102

Claims 1, 2, 3, 5, 7, 8, 10, 11, 12, 14, 17, 19 and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by European Patent Application Publication Number 0 600 611 A2 (hereinafter "Faraydon"). For the ease of the discussion below each respective claim set rejected under 35 U.S.C. § 102(b) is discussed seperately.

IA. Rejection of Claims 1, 2, 3, 5, 7, and 8 under 35 U.S.C. § 102(b):

Claims 1, 2, 3, 5, 7, and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Faraydon. Applicants' respectfully traverse this rejection and contend the Faraydon does not anticipate Claims 1, 2, 3, 5, 7 and 8.

Claims 2, 3, 5, 7, and 8 depend directly or indirectly upon Claim 1, and therefore, incorporate the patentable features of Claim 1.

Claim 1 is directed to a method for managing a number of physical registers. The method is performed in a microprocessor having a number of physical registers. The method includes a step of providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. The destination operand identifying where data resulting from an operation is to be stored. The method further includes, amongst other steps, a step of storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not anticipate Claim 1.

The Faraydon reference is directed to a super scalar computer system that includes a set of general purpose registers. Each register includes a field for setting a lock bit to prevent a read or write operation from occuring before the formal state of the processor updates. The super scalar computer system disclosed by the Faraydon reference further includes a number of collision vector tables (CVT). Each CVT table has a base address and a number of individual rows and columns. Each CVT row entry has three fields, one to hold the physical address of a register for renaming, the second to hold the programmers architectured registered address as defined in the original instruction, and the third field holding flags or indicators necessary for the specific implementation. For example, there can be three flag bits, individiually indicating that the entry is in use, the instruction has been executed, and that the instruction has caused an interupt.

Each CVT table of the Faraydon reference identifies in a <u>first</u> column information identifying available physical registers that are <u>free</u> to be assigned as a destination operand for instructions executing on the microprocessor. *See*, Figures 6-12 and page six, lines 27-28 of Faraydon. Further, each CVT table includes a row which stores a physical register assignment noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. *See*, Figures 8-12 and page 6, lines 51-52 of Faraydon.

More specifically, the Faraydon references discloses one structure that holds information identifying available physical registers that are free to be assigned as destination operands for instructions executing on the registers and stores a physical register assignment noting that the selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the processor. That one structure is a CVT table. *See*, Figure 9 and page 6, line 58 to page 7, line 1 of Faraydon. That is, in the third column of the CVT tables disclosed by Faraydon a flag bit is used to indicate that the physical register identified in the first column of the CVT table is assigned as an operation operand for a selected instruction.

In contrast, to the Faraydon reference, Claim 1 recites a step of providing a *first* structure holding information identifing available physical registers that are free to be assigned as destination operand for instructions executing on the microprocessor. Claim 1 further recites a step of storing a physical register assignment in a *second* structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not disclose such features. The Faraydon reference discloses one structure, a CVT table to hold information identifying physical registers free to be assigned as destination operand for instructions executing on the microprocessor (i.e., first column of a CVT table) and a physical register assignment (i.e., second column of the CVT table) and a note indicating the selected physical register is assigned as a destination operand for a slected instruction (i.e., third column of the CVT table). The Faraydon reference does not anticipate Claim 1.

The Examiner submits that the general purpose registers (GPR)(16) and the associated lock bits (17) disclose by Faraydon correspond to the first structure of Claim 1. Applicants respectfully disagree. To the contrary, the lock bits associated with the physical locations of general purpose registers (16) disclosed by Faraydon do not identify available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. Rather, the lock bits of Faraydon are used to prevent the reading or writing to physical registers before an instruction has retired to ensure proper data dependencies. For example, as shown in Figure 8 of Faraydon, the first four registers (00-03) of the illustrated GPR each have a lock bit value of (0) and the fifth register (04) has a lock bit value of (1). Nevertheless, the second register (01) and the third register

(02), which are source registers that hold data for an instruction and are not free to be assigned as a destination operand for instructions executing on the microprocessor. Hence, following the Examiner's assertions then a lock bit of value (0) indicates a free register available as a destination of an operand leaving source registers (01) and (02) available as destinations for an operand. Furthermore, the Faraydon reference discloses that the lock bits are used to control dependencies between source registers and destination registers and are not meant to indicate an available physical register. That function in the Faraydon reference is carried out by the CVT table. Accordingly, the Faraydon reference does not anticipate Claim 1.

Accordingly, Applicant's respectfully request the Examiner to reconsider and withdraw the rejection of Claims 1, 2, 3, 5, 7, and 8 under 35 U.S.C. §102(b).

IB. Rejection of Claims 10, 11, 12, 14, and 17 under 35 U.S.C. § 102(b):

Claims 10, 11, 12, 14, and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Faraydon. Applicants' respectfully traverse this rejection and contend the Faraydon does not anticipate Claims 10, 11, 12, 14, and 17.

Claims 11, 12, 14, and 17 depend directly or indirectly upon Claim 10, and therefore, incorporate the patentable features of Claim 10.

Claim 10 is directed to a method for managing a number of physical registers. The method is performed in a microprocessor having a number of physical registers. The method includes a step of providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. The destination operand identifying where data resulting from an operation is to be stored. The method further includes, amongst other steps, a step of storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not anticipate Claim 10.

The Faraydon reference is directed to a super scalar computer system that includes a set of general purpose registers. Each register includes a field for setting a lock bit to prevent a read or write operation from occuring before the formal state of the processor updates. The super scalar computer system disclosed by the Faraydon reference further includes a number of collision vector tables (CVT). Each CVT table has a base address and a number of individual rows and columns. Each CVT row entry has three fields, one to hold the physical address of a register for renaming, the second to hold the programmers architectured registered address as defined in the original instruction, and the third field holding flags or indicators necessary for the specific implementation. For example, there can be three flag bits, individiually indicating that the entry is in use, the instruction has been executed, and that the instruction has caused an interupt.

Each CVT table of the Faraydon reference identifies in a first column information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. *See*, Figures 6-12 and page six, lines 27-28 of Faraydon. Further, each CVT table includes a row which stores a physical register assignment noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. *See*, Figures 8-12 and page 6, lines 51-52 of Faraydon.

More specifically, the Faraydon references discloses one structure that holds information identifying available physical registers that are free to be assigned as destination operands for instructions executing on the registers and stores a physical register assignment noting that the selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the processor. That one structure is a CVT table. *See*, Figure 9 and page 6, line 58 to page 7, line 1 of Faraydon. That is, in the third column of the CVT tables disclosed by Faraydon a flag bit is used to indicate that the physical register identified in the first column of the CVT table is assigned as an operation operand for a selected instruction.

In contrast, to the Faraydon reference, Claim 10 recites a step of providing a *first* structure holding information identifing available physical registers that are free to be assigned as destination operand for instructions executing on the microprocessor. Claim 10 further recites a step of storing

a physical register assignment in a *second* structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not disclose such features. The Faraydon reference discloses one structure, a CVT table to hold information identifying physical registers free to be assigned as destination operand for instructions executing on the microprocessor (i.e., first column of a CVT table) and a physical register assignment (i.e., second column of the CVT table) and a note indicating the selected physical register is assigned as a destination operand for a slected instruction (i.e., third column of the CVT table). The Faraydon reference does not anticipate Claim 10.

The Examiner submits that the general purpose registers (GPR)(16) and the associated lock bits (17) disclose by Faraydon correspond to the first structure of Claim 10. Applicants respectfully disagree. To the contrary, the lock bits associated with the physical locations of general purpose registers (16) disclosed by Faraydon do not identify available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. Rather, the lock bits of Faraydon are used to prevent the reading or writing to physical registers before an instruction has retired to ensure proper data dependencies. For example, as shown in Figure 8 of Faraydon, the first four registers (00-03) of the illustrated GPR each have a lock bit value of (0) and the fifth register (04) has a lock bit value of (1). Nevertheless, the second register (01) and the third register (02), which are source registers that hold data for an instruction and are not free to be assigned as a destination operand for instructions executing on the microprocessor. Hence, following the Examiner's assertions then a lock bit of value (0) indicates a free register available as a destination of an operand leaving source registers (01) and (02) available as destinations for an operand. Furthermore, the Faraydon reference discloses that the lock bits are used to control dependencies between source registers and destination registers and are not meant to indicate an available physical register. That function in the Faraydon reference is carried out by the CVT table. Accordingly, the Faraydon reference does not anticipate Claim 10.

Accordingly, Applicant's respectfully request the Examiner to reconsider and withdraw the rejection of Claims 10, 11, 12, 14, and 17 under 35 U.S.C. §102(b).

IC. Rejection of Claim 19 under 35 U.S.C. § 102(b):

Claim 19 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Faraydon. Applicants' respectfully traverse this rejection and contend the Faraydon does not anticipate Claim 19.

Claim 19 is directed to a microprocessor system with a plurality of physical registers for managing a plurality of physical register assignments. The microprocessor system includes, amongst other features, a first module and a second module. The first module is for providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. The destination operand identifying where data resulting from an operation is to be stored. the a second module is for storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not anticipate Claim 19.

The Faraydon reference is directed to a super scalar computer system that includes a set of general purpose registers. Each register includes a field for setting a lock bit to prevent a read or write operation from occuring before the formal state of the processor updates. The super scalar computer system disclosed by the Faraydon reference further includes a number of collision vector tables (CVT). Each CVT table has a base address and a number of individual rows and columns. Each CVT row entry has three fields, one to hold the physical address of a register for renaming, the second to hold the programmers architectured registered address as defined in the original instruction, and the third field holding flags or indicators necessary for the specific implementation. For example, there can be three flag bits, individiually indicating that the entry is in use, the instruction has been executed, and that the instruction has caused an interupt.

Each CVT table of the Faraydon reference identifies in a first column information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. *See*, Figures 6-12 and page six, lines 27-28 of Faraydon. Further, each CVT table includes a row which stores a physical register assignment

noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. *See*, Figures 8-12 and page 6, lines 51-52 of Faraydon.

More specifically, the Faraydon references discloses one structure that holds information identifying available physical registers that are free to be assigned as destination operands for instructions executing on the registers and stores a physical register assignment noting that the selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the processor. That one structure is a CVT table. *See*, Figure 9 and page 6, line 58 to page 7, line 1 of Faraydon. That is, in the third column of the CVT tables disclosed by Faraydon a flag bit is used to indicate that the physical register identified in the first column of the CVT table is assigned as an operation operand for a selected instruction.

In contrast, to the Faraydon reference, Claim 19 recites a *first* module for providing a *first* structure holding information identifing available physical registers that are free to be assigned as destination operand for instructions executing on the microprocessor. Claim 19 further recites a *second* module for storing a physical register assignment in a *second* structure noting that a selected one of the physical registers is assigned as a destination operand for a selected instruction executing on the microprocessor. The Faraydon reference does not disclose such features. The Faraydon reference discloses one structure, a CVT table to hold information identifying physical registers free to be assigned as destination operand for instructions executing on the microprocessor (i.e., first column of a CVT table) and a physical register assignment (i.e., second column of the CVT table) and a note indicating the selected physical register is assigned as a destination operand for a slected instruction (i.e., third column of the CVT table). The Faraydon reference does not anticipate Claim 19.

The Examiner submits that the general purpose registers (GPR)(16) and the associated lock bits (17) disclose by Faraydon correspond to the first structure of Claim 19. Applicants respectfully disagree. To the contrary, the lock bits associated with the physical locations of general purpose registers (16) disclosed by Faraydon do not identify available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor. Rather, the lock

bits of Faraydon are used to prevent the reading or writing to physical registers before an instruction has retired to ensure proper data dependencies. For example, as shown in Figure 8 of Faraydon, the first four registers (00-03) of the illustrated GPR each have a lock bit value of (0) and the fifth register (04) has a lock bit value of (1). Nevertheless, the second register (01) and the third register (02), which are source registers that hold data for an instruction and are not free to be assigned as a destination operand for instructions executing on the microprocessor. Hence, following the Examiner's assertions then a lock bit of value (0) indicates a free register available as a destination of an operand leaving source registers (01) and (02) available as destinations for an operand. Furthermore, the Faraydon reference discloses that the lock bits are used to control dependencies between source registers and destination registers and are not meant to indicate an available physical register. That function in the Faraydon reference is carried out by the CVT table. Accordingly, the Faraydon reference does not anticipate Claim 19.

Accordingly, Applicant's respectfully request the Examiner to reconsider and withdraw the rejection of Claim 19 under 35 U.S.C. §102(b).

ID. Rejection of Claim 21 under 35 U.S.C. § 102(b):

Claim 21 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Faraydon. Applicants' respectfully traverse this rejection and contend the Faraydon does not anticipate Claim 21. Nevertheless, Claim 21 is canceled by this amendment and therefore Applicants consider the rejection of Claim 21 moot.

Accordingly, Applicant's respectfully request the Examiner to reconsider and withdraw the rejection of Claim 21 under 35 U.S.C. §102(b).

Claim Rejections under 35 U.S.C. § 103

Claims 4, 6, 9,13, 15, 18, and 20 stand rejected under 35 U.S.C. § 103(a). Applicants traverse each of these rejections. For the ease of the discussion below each respective claim set rejected under 35 U.S.C. § 103(a) is discussed seperately.

IIA. Rejection of Claim 4 under 35 U.S.C. § 103(a):

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon. Applicants' respectfully traverse this rejections and contend the Faraydon does not teach or suggest each and every element of Claim 4.

Claim 4 depends directly or indirectly on independent Claim 1, and therefore, incorporate the patentable features of Claim 1.

Claim 4 recites the further patentable feature of a microprocessor simultaneously executes multiple threads. The Examiner has taken Offical Notice that threads and the ablility of a processor to execute multiple threads in parallel (simultaneously) is well know and expected in the art. The Examiner states "when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially."

Nonetheless, Applicants' traverse the Examiner's assertion of Official Notice that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known. In support of Applicants' assertion that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known Applicants' contend that the Examiner's reasoning regarding the amount of work that can be performed in parallel versus a single thread. That is, one skilled in the art would recognize that in a multi-thread mode the number of available registers in the processor is shared amongst all of the threads, hence limiting the amount of work do to resource contention. However, in a single thread mode, all available registers can be allocated to the one thread avoiding resource contention and in fact increasing the amount of work the processor can handle. Hence, the Examiner's reasoning underlying the decision to take such notice is unclear and flawed. Hence, Applicants' specifically point out why the noticed fact is not considered to be common knowledge or well known in the art, and further request the Examiner to submit documentary evidence in support of such a finding in any further rejection taken under Official Notice.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 4 under 35 U.S.C. § 103(a).

IIB. Rejection of Claim 13 under 35 U.S.C. § 103(a):

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon. Applicants' respectfully traverse this rejections and contend the Faraydon does not teach or suggest each and every element of Claim 13.

Claim 13 depends directly or indirectly on independent Claim 10, and therefore, incorporate the patentable features of Claim 10.

Claim 13 recites the further patentable feature of a microprocessor simultaneously executes multiple threads. The Examiner has taken Offical Notice that threads and the ablility of a processor to execute multiple threads in parallel (simultaneously) is well know and expected in the art. The Examiner states "when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially."

Nonetheless, Applicants' traverse the Examiner's assertion of Official Notice that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known. In support of Applicants' assertion that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known Applicants' contend that the Examiner's reasoning regarding the amount of work that can be performed in parallel versus a single thread. That is, one skilled in the art would recognize that in a multi-thread mode the number of available registers in the processor is shared amongst all of the threads, hence limiting the amount of work do to resource contention. However, in a single thread mode, all available registers can be allocated to the one thread avoiding resource contention and in fact increasing the amount of work the processor can handle. Hence, the Examiner's reasoning underlying the decision to take such notice is unclear and flawed. Hence, Applicants' specifically point out why the noticed fact is not

considered to be common knowledge or well known in the art, and further request the Examiner to submit documentary evidence in support of such a finding in any further rejection taken under Official Notice.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 13 under 35 U.S.C. § 103(a).

IIC. Rejection of Claim 20 under 35 U.S.C. § 103(a):

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon. Applicants' respectfully traverse this rejections and contend the Faraydon does not teach or suggest each and every element of Claim 20.

Claim 20 depends directly or indirectly on independent Claim 19, and therefore, incorporate the patentable features of Claim 19.

Claim 20 recites the further patentable feature of a microprocessor simultaneously executes multiple threads. The Examiner has taken Offical Notice that threads and the ablility of a processor to execute multiple threads in parallel (simultaneously) is well know and expected in the art. The Examiner states "when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially."

Nonetheless, Applicants' traverse the Examiner's assertion of Official Notice that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known. In support of Applicants' assertion that a microprocessor simultaneously executes multiple threads at the time the invention was made was well known Applicants' contend that the Examiner's reasoning regarding the amount of work that can be performed in parallel versus a single thread. That is, one skilled in the art would recognize that in a multi-thread mode the number of available registers in the processor is shared amongst all of the threads, hence limiting the amount of work do to resource contention. However, in a single thread mode, all available registers can be

allocated to the one thread avoiding resource contention and in fact increasing the amount of work the processor can handle. Hence, the Examiner's reasoning underlying the decision to take such notice is unclear and flawed. Hence, Applicants' specifically point out why the noticed fact is not considered to be common knowledge or well known in the art, and further request the Examiner to submit documentary evidence in support of such a finding in any further rejection taken under Official Notice.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 20 under 35 U.S.C. § 103(a).

IID. Rejection of Claim 6 under 35 U.S.C. § 103(a):

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon in view of U.S. Patent No. 5, 546, 554 of Yung (hereinafter "Yung"). Applicants' respectfully traverse this rejections and contend neither Faraydon nor Yung, alone or in combination, teach or suggest each and every element of Claim 6.

Claim 6 depends directly or indirectly on independent Claim 1, and therefore, incorporate the patentable features of Claim 1.

Yung is cited for teaching or suggesting that the contents of the assigned available physical registers are flushed from the assigned available physical registers. Nevertheless, the Yung reference fails to bridge the factual deficiencies of the Faraydon reference. That is, the Yung reference does not disclose a method for managing a number of physical registers in a microprocessor having a plurality of physical registers as recited in Claim 1. Accordingly, neither Yung nor Faraydon, alone or in combination, detract from the patentability of Claim 6.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 6 under 35 U.S.C. §103(a).

IIE. Rejection of Claim 15 under 35 U.S.C. § 103(a):

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon in view of Yung. Applicants' respectfully traverse this rejections and contend neither Faraydon nor Yung, alone or in combination, teach or suggest each and every element of Claim 15.

Claim 15 depends directly or indirectly on independent Claim 10, and therefore, incorporate the patentable features of Claim 10.

Yung is cited for teaching or suggesting that the contents of the assigned available physical registers are flushed from the assigned available physical registers. Nevertheless, the Yung reference fails to bridge the factual deficiencies of the Faraydon reference. That is, the Yung reference does not disclose a method for managing a number of physical registers in a microprocessor having a plurality of physical registers as recited in Claim 10. Accordingly, neither Yung nor Faraydon, alone or in combination, detract from the patentability of Claim 15.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 15 under 35 U.S.C. §103(a).

IIF. Rejection of Claim 9 under 35 U.S.C. § 103(a):

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon in view of Tanenbaum, Structured Computer Organization, 2nd Edition, 1984, page 11 (hereinafter "Tanenbaum"). Applicants' respectfully traverse this rejections and contend neither Faraydon nor Tanenbaum, alone or in combination, teach or suggest each and every element of Claim 9.

Claim 9 depends directly or indirectly on independent Claim 1, and therefore, incorporate the patentable features of Claim 1.

Tanenbaum is cited for teaching or suggesting that hardware and software are logically equivalent. Nevertheless, although hardware and software may be logically equivalent they are not structurally equivalent. Furthermore, the Tanenbaum reference fails to bridge the factual deficiencies of the Faraydon reference. That is, the Tanenbaum reference does not disclose a method for managing a number of physical registers in a microprocessor having a plurality of physical registers as recited in Claim 1. Accordingly, neither Yung nor Tanenbaum, alone or in combination, detract from the patentability of Claim 9.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 9 under 35 U.S.C. §103(a).

IIE. Rejection of Claim 18 under 35 U.S.C. § 103(a):

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Faraydon in view of Tanenbaum. Applicants' respectfully traverse this rejections and contend neither Faraydon nor Tanenbaum, alone or in combination, teach or suggest each and every element of Claim 18.

Claim 18 depends directly or indirectly on independent Claim 10, and therefore, incorporate the patentable features of Claim 10.

Tanenbaum is cited for teaching or suggesting that hardware and software are logically equivalent. Nevertheless, although hardware and software may be logically equivalent they are not structurally equivalent. Furthermore, the Tanenbaum reference fails to bridge the factual deficiencies of the Faraydon reference. That is, the Tanenbaum reference does not disclose a method for managing a number of physical registers in a microprocessor having a plurality of physical registers as recited in Claim 10. Accordingly, neither Yung nor Tanenbaum, alone or in combination, detract from the patentability of Claim 18.

Accordingly, applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 18 under 35 U.S.C. §103(a).

CONCLUSION

In view of the remarks set forth above, Applicant contends that Claims 1-20 are presently pending in this application, are patentable an in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

Dated: September 22, 2004

Respectfully submitted,

By David R Burns

David R. Burns
Registration No.: 46,590
LAHIVE & COCKFIELD, LLP
28 State Street
Boston, Massachusetts 02109
(617) 227-7400
(617) 742-4214 (Fax)
Attorney For Applicant

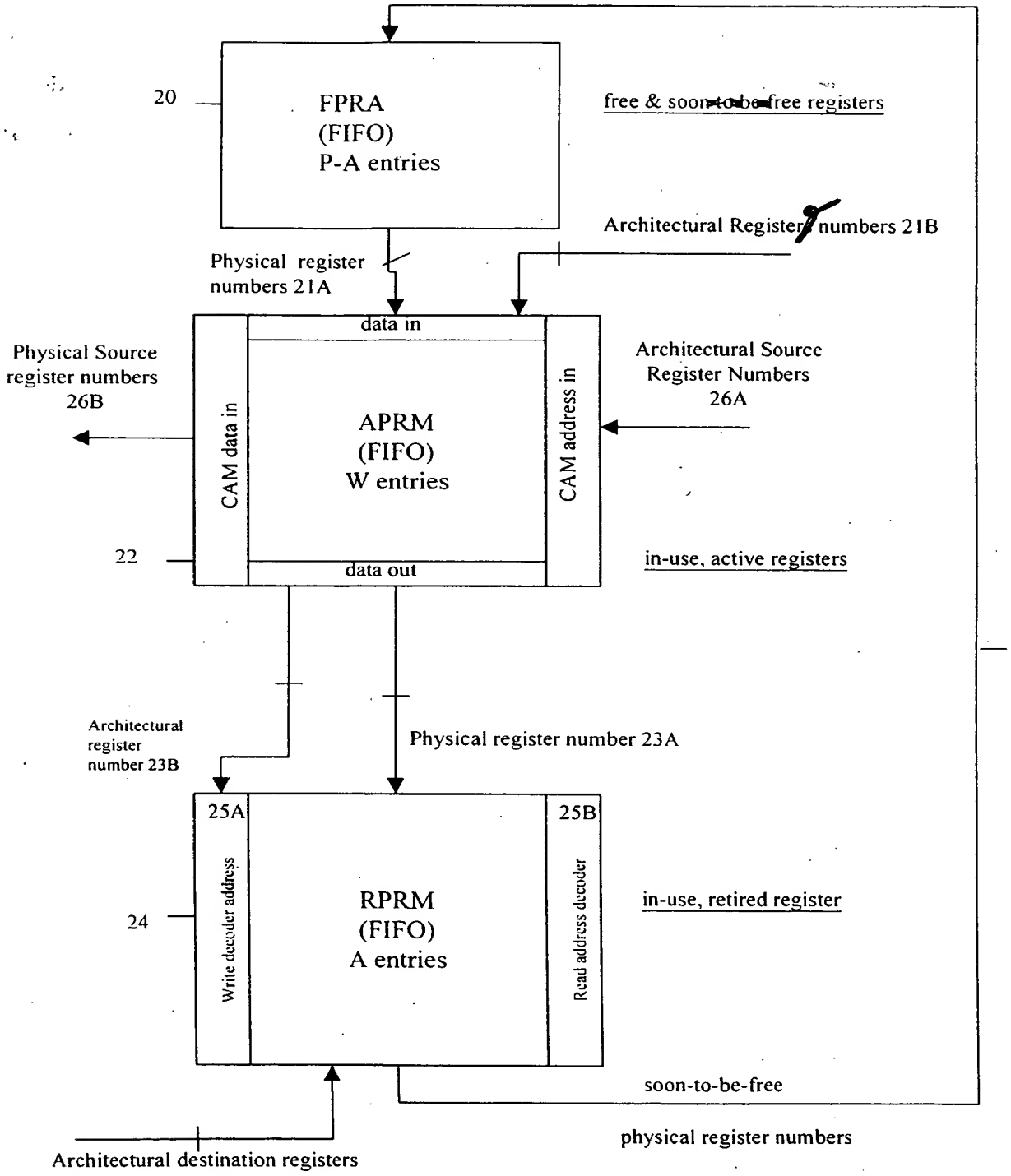

FIGURE 2B

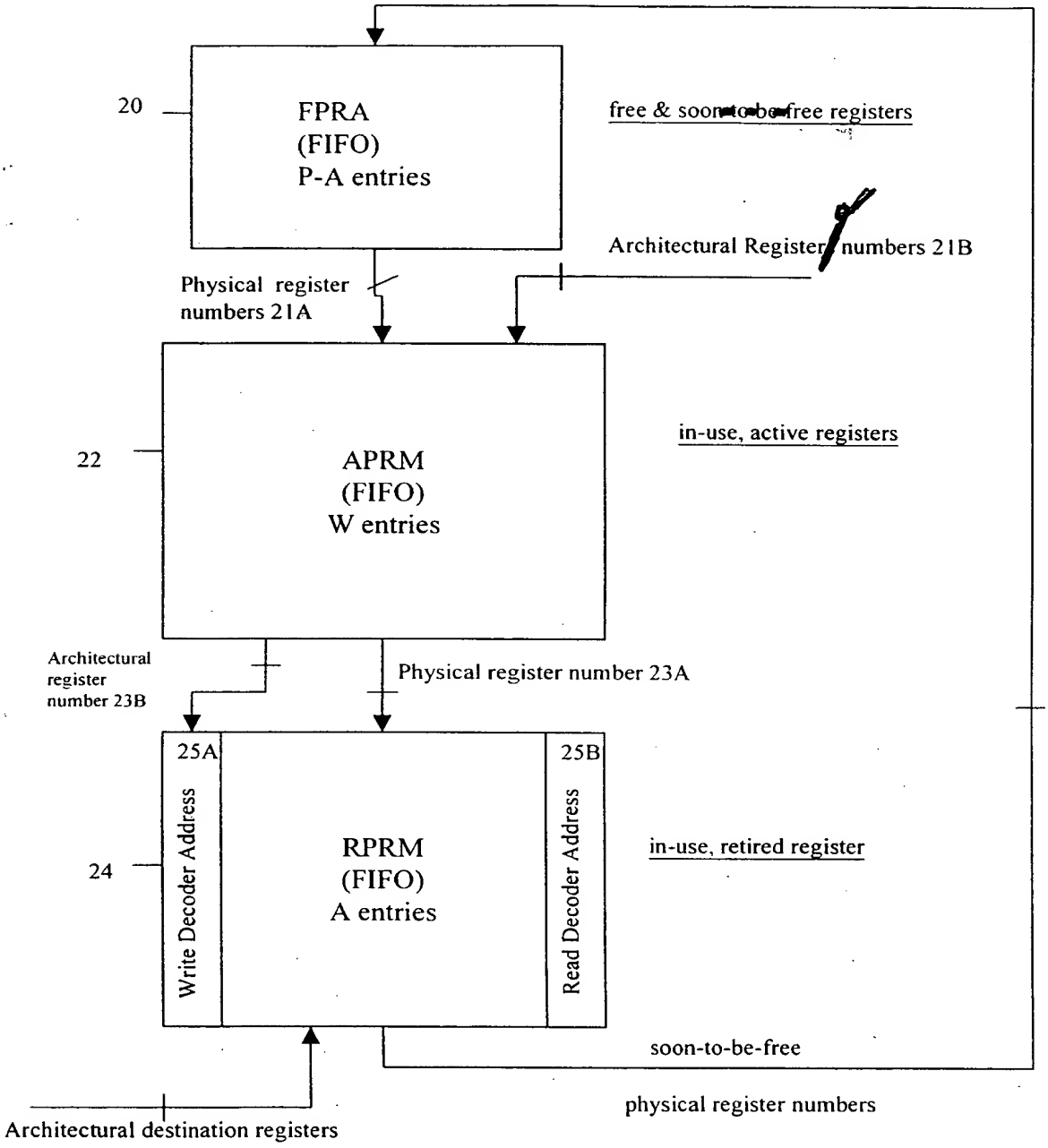

FIGURE 2A

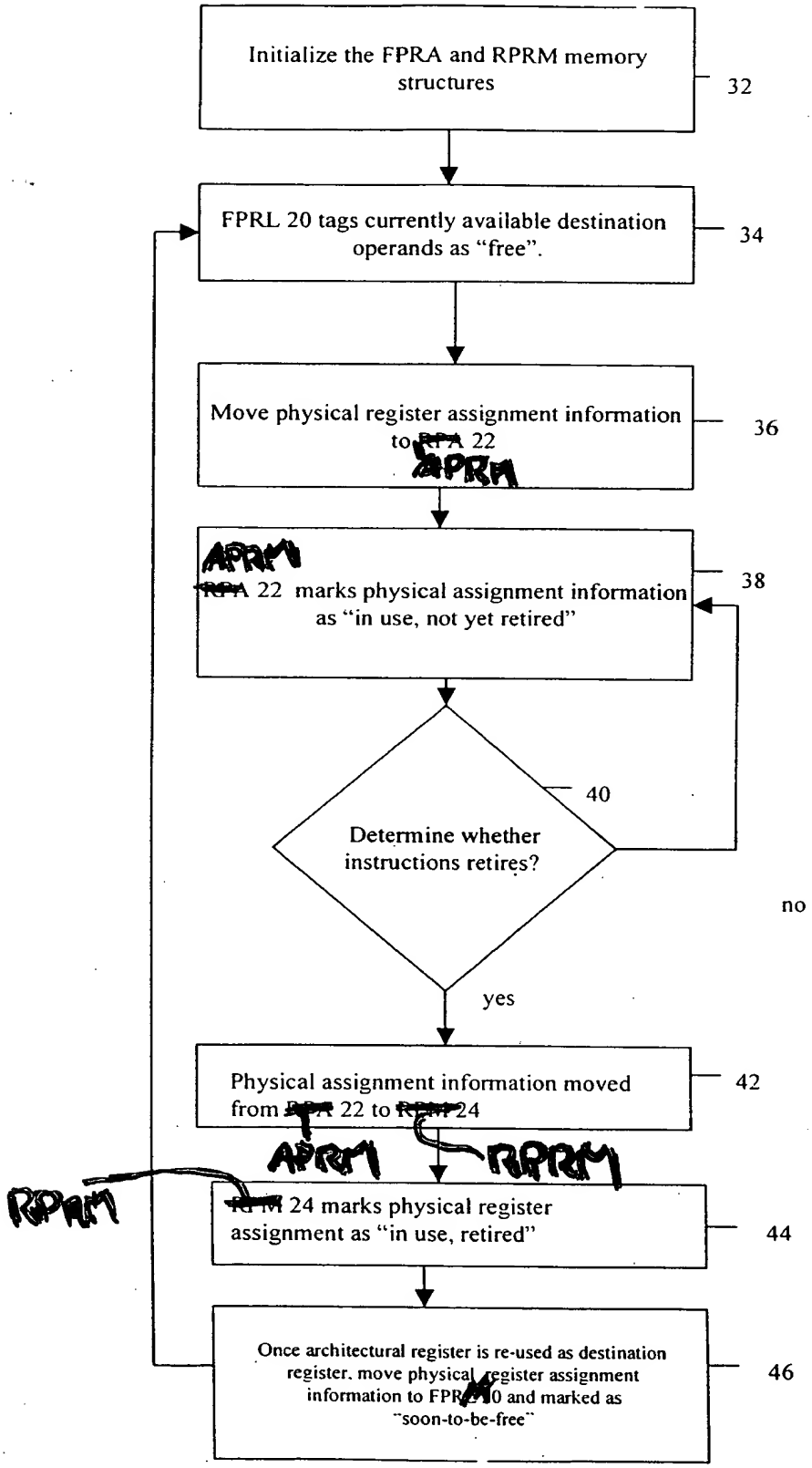

FIGURE 3